IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Wood et al.

Patent No.: 6,036,872
Serial No.: 09/052,645

Examiner: N. Nguyen

Issued: March 14, 2000
Filed: March 31, 1998

Group Art Unit: 1763

For: METHOD OF MAKING A WAFER-PAIR HAVING SEALED CHAMBERS

Docket No.: 1100.1138101 (H16-17400)

PRELIMINARY AMENDMENT

BOX REISSUE
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CERTIFICATE UNDER 37 C.F.R. 1.10: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, "Express Mail Post Office to Addressee" having an Express Mail mailing label number of: EL901546446US, in an envelope addressed to: U.S. Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202 on this 3rd day of December, 2001.

By Jolene Alger
Jolene Alger

Sir:

Please amend the above-captioned application as follows:

In the Claims

Please add newly presented claims 25-55 as follows:

25. A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:

growing a thermal layer on a first side of a first wafer;

depositing a nitride layer on the thermal layer;

depositing, patterning and removing portions of first metal layer on the nitride

layer for a plurality of devices;

depositing, patterning and removing portions of a second metal layer on the nitride and first metal layers for the plurality of devices;

patterning and removing material from the first wafer and layers on the first side of the first wafer and from a second side of the first wafer to make a plurality of pump-out ports through the first wafer and layers on the first wafer;

masking and removing material from a first side of a second wafer to form a plurality of recesses in the first side of the second wafer;

forming a sealing ring on the first side of the second wafer around each of the plurality of recesses; and

positioning the first side of the first wafer next to the first side of the second wafer; and wherein:

each sealing ring is in contact with at least one of the layers on the first side of the first wafer;

each recess of the plurality of recesses results in a chamber containing at least one device of the plurality of devices;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and

the first and second wafers are effectively a bonded together set of wafers.

26. The method of claim 25, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via the at least one pump-out port; and

depositing a layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first wafer, wherein each chamber is sealed from the environment.

27. The method of claim 26, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first wafer.

28. The method of claim 27, further comprising coating the second wafer with antireflection material.

29. The method of claim 28, wherein the second wafer is made from a material that is at least substantially transparent to light in the infrared spectrum.

30. The method of claim 29, wherein the plurality of devices comprise thermoelectric detectors.

31. The method of claim 30, wherein the plurality of devices comprise bolometers.

32. A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

growing a first thermal layer on a first side of a first wafer;

depositing a nitride layer on the first thermal layer;

depositing and patterning a first metal layer on the nitride layer for at least one device;

depositing and patterning a second metal layer on the nitride layer and the first metal layer for the at least one device;

patterning and removing material from the first wafer and layers on the first side of the first wafer and from a second side of the first wafer to make a pump-out port through the first wafer and the layers on the first wafer;

masking and removing material from a first side of a second wafer, to form a recess in the first side of the second wafer;

forming a sealing ring on the first side of the second wafer around the recess;

positioning the first side of the first wafer next to the first side of the second wafer; and

wherein:

the sealing ring is in contact with at least one of the layers on the first side of the first wafer;

the at least one device is within the recess resulting in a chamber containing the at least one device;

the pump-out port is within the sealing ring; and

the first and second wafers are effectively a bonded together set of wafers.

33. The method of claim 32, further comprising:

placing the bonded together set of wafers in an environment of a vacuum wherein a vacuum occurs in the chamber via the pump-out port; and

depositing a layer of material on the second side of the first wafer and the pump-out port on the second side of the first wafer, wherein the chamber is sealed from the environment.

34. The method of claim 33, further comprising baking out the bonded together set of wafers prior to depositing the layer of material on the second side of the first wafer and the pump-out port on the second side of the first wafer.

35. The method of claim 34, wherein the at least one device is a detector.

36. The method of claim 35, wherein the at least one device is a thermoelectric detector.

37. The method of claim 34, wherein the at least one device is an emitter.

38. A method for making a wafer-pair having sealed chambers, comprising:

patterning and removing material from a first wafer to make a plurality of pump-out ports through the first wafer;

masking and removing material from a first side of a second wafer to form a plurality of recesses in the first side of the second wafer;

forming a sealing ring on a first side of the first wafer or the first side of the second wafer such that the sealing ring extends around each of the plurality of recesses; and

positioning the first side of the first wafer next to the first side of the second wafer; and

wherein:

each sealing ring is in contact with the first side of the first wafer and the first side of the second wafer

each recess of the plurality of recesses results in a chamber;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and

the first and second wafers are effectively a bonded together set of wafers.

39. The method of claim 38, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via a pump-out port; and

depositing a layer of material on a second side of the first wafer to seal the plurality of pump-out out ports from the second side of the first wafer, wherein each chamber is sealed from the environment.

40. The method of claim 39, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer.

41. The method of claim 40, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

42. The method of claim 40, wherein the one or more sealed chambers contains one or more devices.

43. The method of claim 38, further comprising:

placing the set of wafers in an environment of a gas wherein the gas enters each chamber via a pump-out port; and

depositing a layer of material on a second side of the first wafer to seal the plurality of pump-out out ports from the second side of the first wafer, wherein each chamber is sealed from an ambient environment.

44. A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer and a second wafer;

forming one or more pump-out ports through the first wafer;

positioning a first side of the first wafer next to a first side of the second wafer with a sealing ring therebetween, the first wafer, the second wafer and the sealing ring forming a chamber, with the pump-out port of the first wafer in fluid communication with the chamber; and

plugging the pump out port to seal the chamber.

45. A method according to claim 44 further comprising the step of:

making a recess in the first side of the first wafer and/or the first side of the second wafer, wherein the recess is in registration with the chamber.

46. A method according to claim 44 further comprising the step of:

providing one or more devices in or on the first side of the first wafer and/or the first side of the second wafer before the positioning step.

47. A method according to claim 46 wherein the one or more devices are in registration with the chamber.

48. A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer and a second wafer;

forming one or more pump-out ports through the first wafer;

making a recess in a first side of the first wafer and/or a first side of the second wafer;

positioning the first side of the first wafer next to the first side of the second wafer, the first wafer and the second wafer forming a chamber that is at least partially defined by the recess, with the pump-out port of the first wafer in fluid communication with the chamber; and

plugging the pump out port to seal the chamber.

49. A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer having a first side, with one or more bond pads on the first side;

providing a second wafer;

forming one or more bond-pad holes through the second wafer;

positioning the first side of the first wafer next to a first side of the second wafer with a sealing ring therebetween; the first wafer, the second wafer and the sealing ring forming a chamber, the first wafer and second wafer being aligned so that the bond-pad holes are in registration with the one or more bond pads on the first wafer; and

the first and second wafers are effectively a bonded together set of wafers.

50. A bonded wafer pair, comprising:

a first wafer;

a second wafer;

the first wafer having one or more pump-out ports through the first wafer;

the first side of the first wafer bonded to a first side of the second wafer via a sealing ring; the first wafer, the second wafer and the sealing ring forming a chamber, with the pump-out port of the first wafer in fluid communication with the chamber; and

a plug for plugging the pump out port.

51. A bonded wafer pair according to claim 50 further comprising a recess in the first side of the first wafer and/or the first side of the second wafer, wherein the recess is in registration with the chamber.

52. A bonded wafer pair according to claim 50 further comprising one or more devices in or on the first side of the first wafer and/or the first side of the second wafer.

53. A bonded wafer pair according to claim 52 wherein the one or more devices are in registration with the chamber.

54. A bonded wafer pair having a sealed chamber, comprising:

a first wafer;

a second wafer bonded to the first wafer;

one or more pump-out ports through the first wafer;

a recess in a first side of the first wafer and/or a first side of the second wafer;

the first wafer and the second wafer forming a chamber that includes the recess, with the pump-out port of the first wafer in fluid communication with the chamber; and

one or more plugs for plugging the one or more pump out ports to seal the chamber.

55. A bonded wafer pair, comprising:

a first wafer having a first side, with one or more bond pads on the first side;

a second wafer, with one or more bond-pad holes through the second wafer;

the first side of the first wafer bonded to a first side of the second wafer with a sealing ring therebetween, the first wafer and second wafer being aligned so that the bond-pad holes are in registration with the one or more bond pads on the first wafer; and

the first wafer, the second wafer and the sealing ring forming a chamber.

Remarks

Applicants request that the preceding claim amendments be made of record and fully considered before the first Office Action on the merits. Any inquiry regarding this matter may be directed to the undersigned representative at (612) 677-9050.

Respectfully submitted,

R. Andrew Wood et al.

By their attorney,

Date: December 3, 2001

Brian N. Tufte, Reg. No. 38,638
CROMPTON, SEAGER & TUFTE, LLC
331 Second Avenue South, Suite 895
Minneapolis, Minnesota 55401-2246
Telephone: (612) 677-9050
Facsimile: (612) 359-9349

PATENT

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For: METHOD OF MAKING A WAFER-PAIR HAVING SEALED CHAMBERS

Docket No.: 1100.1138101 (H16-17400)

STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES (37 CFR 1.173(C))

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By ______________________
Jolene Alger

Sir:

In accordance with 37 CFR §1.173(c)): "Whenever there is an amendment to the claims pursuant to paragraph (b) of this section, there must also be supplied, on pages separate from the pages containing the changes, the status (i.e., pending or cancelled), as of the date of the amendment, of all patent claims and of all added claims, and an

explanation of the support in the disclosure of the patent for the changes made to the claims."

The status of the claims as a result of the amendment submitted herewith is:

Claims 25-55 have been added.

The support in the disclosure of the patent for the changes made to the claims and for the claims added is as follows:

Claim #	Claim Phrase	Examples of Locations in Specification that disclose the claimed element.
25	A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:	Column 2 lines 10-12: "FIGS. 1a, 1b and 2 show an illustration of a device 10 having a vacuum pump-out port 11 and a deposited plug final vacuum seal 12."
	growing a thermal layer on a first side of a first wafer;	Column 2 lines 49-51: "A 1000 angstroms of a thermal SiO_2 layer 24 is grown on the front of wafer 13 in FIG. 4B."
	depositing a nitride layer on the thermal layer;	Column 2 lines 51-53: "A layer 25 of 2000 angstroms of Si_3N_4 (bottom bridge nitride) is deposited on layer 24 in FIG. 4c."
	depositing, patterning and removing portions of first metal layer on the nitride layer for a plurality of devices;	Column 2 lines 53-56: "The first metal NiFe (60:40) of a thermocouple is deposited as a 1100 angstrom layer 26 on layer 25 and then first metal layer 26 is patterned with a first mask by ion milling resulting in the layout of FIG. 4d."
	depositing, patterning and removing portions of a second metal layer on the nitride and first metal layers for the plurality of devices;	Column 2 lines 57-60: "For the second metal of the thermocouple detectors, a thousand angstrom layer 27 of chromium is deposited on layers 25 and 26. Layer 27 in FIG. 4e is patterned with a second mask by ion milling and wet etching."
	patterning and removing material from the first wafer and layers on the first side of the first wafer and from a second side of the first wafer to make a plurality of pump-out ports through the first wafer and layers on the first wafer;	"Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." (Column 2 line 68 to column 3 line 1). "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m." (Column 3 lines 6-11).

	masking and removing material from a first side of a second wafer to form a plurality of recesses in the first side of the second wafer;	"Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si_3N_4 in FIG. 5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO_2 layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37). "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41).
	forming a sealing ring on the first side of the second wafer around each of the plurality of recesses; and	"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50).
	positioning the first side of the first wafer next to the first side of the second wafer; and wherein:	"Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60).
	each sealing ring is in contact with at least one of the layers on the first side of the first wafer;	"Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure." (Column 3 lines 62-63)
	each recess of the plurality of recesses results in a chamber containing at least one device of the plurality of devices;	In describing Figures 1a, 1b, and 2, "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20.) Further, a plurality of such recesses are shown in Figure 3: "FIG. 3 shows a wafer 20 having multiple chips 10 having a wafer-to-wafer sealing of the same material for multiple cavities." (Column 2 lines 28-30). Further, in describing a nearly finished product, "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17)
	each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and	As shown in Figures 1a and 1b. As noted in Column 2 lines 3 0-31, "Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." Column 3 lines 42-50 note that a solder ring pattern (a sealing ring) encircles the recess. Column 4 lines 15-17 notes that each chip has its own sealed chamber.
	the first and second wafers are effectively a	"Wafers 13 and 14 are adhered together at a solder seal ring 15." (Column 2 lines 15-16).

	bonded together set of wafers.	"The present wafers 13 and 14, after bonding and sealing, may be sawed into individual chips without breakage since the sealed top cap protects the fragile microstructure devices 17. Further, the plug will not be disturbed since it is a deposited layer 12 rather than some dislodgable solder ball or plug." (Column 2 lines 37-42) "The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 60-68). "Bonded wafer pair 13 and 14 . . ." (Column 4 line 1) "Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment." (Column 4 lines 13-15).
	The method of claim 25, further comprising: placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via the at least one pump-out port; and	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 30-34). "Wafer pair 13 and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum. The wafer pair 13 and 14 is cooled down but the environment about the wafer pair is kept at the desired vacuum. Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged. Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment. Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 4-17).
	depositing a layer of material on the second	"Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby

	side of the first wafer and the plurality of pump-out ports on the second side of the first wafer, wherein each chamber is sealed from the environment.	close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged." (Column 4 lines 9-13).
27	The method of claim 26, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first wafer.	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 30-34). "Wafer pair 13 and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum." (Column 4 lines 4-7).
28	The method of claim 27, further comprising coating the second wafer with antireflection material.	"radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 19- 20). "Antireflective coating 38 is applied to wafer 14." (Column 3 line 42).
29	The method of claim 28, wherein the second wafer is made from a material that is at least substantially transparent to light in the infrared spectrum	"Further variations on this theme include top cap wafer 14 composed of Germanium for better IR transmission or ZnSe for broadband transmission (i.e., visible and IR)or other optical window materials for application specific optical bandpass behavior." (Column 4 lines 18-22).
30	The method of claim 29, wherein the plurality of devices comprise thermoelectric detectors	"The chamber may enclose at least one device such as a thermoelectric sensor, bolometer, emitter or other kind of device." (Abstract). "Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58).
31	The method of claim 30, wherein the plurality of devices comprise bolometers	"The chamber may enclose at least one device such as a thermoelectric sensor, bolometer, emitter or other kind of device." (Abstract). "Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58). "Detector wafer 13 may have infrared bolometer arrays with readout electronics integrated into the wafer." (Column 4 lines 26-28).
32	A method for making a	Column 2 lines 10-12: "FIGS. 1a, 1b and 2 show an

	wafer-pair having at least one deposited layer plugged sealed chamber, comprising:	illustration of a device 10 having a vacuum pump-out port 11 and a deposited plug final vacuum seal 12."
	growing a first thermal layer on a first side of a first wafer;	Column 2 lines 49-51: "A 1000 angstroms of a thermal SiO_2 layer 24 is grown on the front of wafer 13 in FIG. 4B."
	depositing a nitride layer on the first thermal layer;	Column 2 lines 51-53: "A layer 25 of 2000 angstroms of Si_3N_4 (bottom bridge nitride) is deposited on layer 24 in FIG. 4c."
	depositing and patterning a first metal layer on the nitride layer for at least one device;	Column 2 lines 53-56: "The first metal NiFe (60:40) of a thermocouple is deposited as a 1100 angstrom layer 26 on layer 25 and then first metal layer 26 is patterned with a first mask by ion milling resulting in the layout of FIG. 4d."
	depositing and patterning a second metal layer on the nitride layer and the first metal layer for the at least one device;	Column 2 lines 57-60: "For the second metal of the thermocouple detectors, a thousand angstrom layer 27 of chromium is deposited on layers 25 and 26. Layer 27 in FIG. 4e is patterned with a second mask by ion milling and wet etching."
	patterning and removing material from the first wafer and layers on the first side of the first wafer and from a second side of the first wafer to make a pump-out port through the first wafer and the layers on the first wafer;	Column 2 line 68 to column 3 line 1: "Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." Column 3 lines 6-11: "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m."
	masking and removing material from a first side of a second wafer, to form a recess in the first side of the second wafer;	Column 3 lines 29-31: "Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si_3N_4 in FIG. 5b." Column 3 lines 35-37: "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO_2 layer 37a in FIG. 5d by buffered oxide etch." Column 3 lines 39-41: "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14."
	forming a sealing ring on the first side of the second wafer around the recess;	"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f."

		(Column 3 lines 41-50)
	positioning the first side of the first wafer next to the first side of the second wafer; and wherein:	"Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60)
	the sealing ring is in contact with at least one of the layers on the first side of the first wafer;	"Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure." (Column 3 lines 62-63)
	the at least one device is within the recess resulting in a chamber containing the at least one device;	In describing Figures 1a, 1b, and 2, "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20.) Further, a plurality of such recesses are shown in Figure 3: "FIG. 3 shows a wafer 20 having multiple chips 10 having a wafer-to-wafer sealing of the same material for multiple cavities." (Column 2 lines 28-30). Further, in describing a nearly finished product, "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17)
	the pump-out port is within the sealing ring; and	As shown in Figures 1a, 1b, and 2. Also described: "Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." (Column 2 lines 30-31).
	the first and second wafers are effectively a bonded together set of wafers.	"Wafers 13 and 14 are adhered together at a solder seal ring 15." (Column 2 lines 15-16). "The present wafers 13 and 14, after bonding and sealing, may be sawed into individual chips without breakage since the sealed top cap protects the fragile microstructure devices 17. Further, the plug will not be disturbed since it is a deposited layer 12 rather than some dislodgable solder ball or plug." (Column 2 lines 37-42) "The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers

		13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 60-68). "Bonded wafer pair 13 and 14 . . ." (Column 4 line 1) "Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment." (Column 4 lines 13-15).
33	The method of claim 32, further comprising: placing the bonded together set of wafers in an environment of a vacuum wherein a vacuum occurs in the chamber via the pump-out port; and	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 30-34). "Wafer pair 13 and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum. The wafer pair 13 and 14 is cooled down but the environment about the wafer pair is kept at the desired vacuum. Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged. Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment. Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 4-17).
	depositing a layer of material on the second side of the first wafer and the pump-out port on the second side of the first wafer, wherein the chamber is sealed from the environment.	"Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged." (Column 4 lines 9-13).
34	The method of claim 33, further comprising baking out the bonded together set of wafers prior to depositing the layer of material on the second side of the first wafer and the pump-out port on the second side of the first wafer.	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 30-34). "Wafer pair 13 and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum." (Column 4 lines 4-7).
35	The method of claim 34, wherein the at least one device is a detector.	"The chamber may enclose at least one device such as a thermoelectric sensor, bolometer, emitter or other kind of device." (Abstract).

		"Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58). "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20).
36	The method of claim 35, wherein the at least one device is a thermoelectric detector.	"The chamber may enclose at least one device such as a thermoelectric sensor, bolometer, emitter or other kind of device." (Abstract). "Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58).
37	The method of claim 34, wherein the at least one device is an emitter.	"The chamber may enclose at least one device such as a thermoelectric sensor, bolometer, emitter or other kind of device." (Abstract). "Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58).
38	A method for making a wafer-pair having sealed chambers, comprising: patterning and removing material from the first wafer to make a plurality of pump-out ports through the first wafer;	Column 2 line 68 to column 3 line 1: "Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." Column 3 lines 6-11: "Plastma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 perent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m."
	masking and removing material from a first side of a second wafer to form a plurality of recesses in the first side of the second wafer;	Column 3 lines 29-31: "Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si_3N_4 in FIG. 5b." Column 3 lines 35-37: "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO_2 layer 37a in FIG. 5d by buffered oxide etch." Column 3 lines 39-41: "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14."
	forming a sealing ring on a first side of the first wafer or the first side of the second wafer such that the sealing ring extends around each of the plurality of recesses; and	"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50). See also Figure 1b where seal ring 15 extends around recess 16.

	positioning the first side of the first wafer next to the first side of the second wafer; and	"Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60)
	wherein: each sealing ring is in contact with the first side of the first wafer and the first side of the second wafer	"Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure." (Column 3 lines 62-63)
	each recess of the plurality of recesses results in a chamber;	In describing Figures 1a, 1b, and 2, "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20.) Further, a plurality of such recesses are shown in Figure 3: "FIG. 3 shows a wafer 20 having multiple chips 10 having a wafer-to-wafer sealing of the same material for multiple cavities." (Column 2 lines 28-30). Further, in describing a nearly finished product, "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17)
	each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and	As shown in Figures 1a and 1b. As noted in Column 2 lines 30-31, "Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." Column 3 lines 42-50 note that a solder ring pattern (a sealing ring) encircles the recess. Column 4 lines 15-17 notes that each chip has its own sealed chamber.
	the first and second wafers are effectively a bonded together set of wafers.	"Wafers 13 and 14 are adhered together at a solder seal ring 15." (Column 2 lines 15-16). "The present wafers 13 and 14, after bonding and sealing, may be sawed into individual chips without breakage since the sealed top cap protects the fragile microstructure devices 17. Further, the plug will not be disturbed since it is a deposited layer 12 rather than some dislodgable solder ball or plug." (Column 2 lines 37-42) "The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which

		takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 60-68). "Bonded wafer pair 13 and 14 . . ." (Column 4 line 1) "Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment." (Column 4 lines 13-15).
39	The method of claim 38, further comprising: placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via a pump-out port; and	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 30-34). "Wafer pair 13 and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum. The wafer pair 13 and 14 is cooled down but the environment about the wafer pair is kept at the desired vacuum. Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged. Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment. Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 4-17).
	depositing a layer of material on a second side of the first wafer to seal the plurality of pump-out out ports from the second side of the first wafer, wherein each chamber is sealed from the environment.	"Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged." (Column 4 lines 9-13).
40	The method of claim 39, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer.	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 30-34). "Wafer pair 13 and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum." (Column 4 lines 4-7).
41	The method of claim 40, wherein the set of	"The present wafers 13 and 14, after bonding and sealing, may be sawed into individual chips without breakage since the

	wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.	sealed top cap protects the fragile microstructure devices 17. Further, the plug will not be disturbed since it is a deposited layer 12 rather than some dislodgable solder ball or plug." (Column 2 lines 37-42). "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17).
42	The method of claim 40, wherein the one or more sealed chambers contains one or more devices.	"The procedure here has been implemented and resulted in vacuum levels below 10 millitorr of residual pressure as measured by pressure sensors within the cavity." (Column 1 lines 41-44). "Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58). "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20). "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17). "Top cap wafer 14 may have integrated components built in or on the surface in addition to those on the detector wafer 13. Detector wafer 13 having a diaphragm pressure sensor integrated into it, the sealed chamber then forms a vacuum pressure reference. Detector wafer 13 may have infrared bolometer arrays with readout electronics integrated into the wafer. Detector wafer 13 may have moving parts to be sealed in a chamber for other functional purposes." (Column 4 lines 22-30).
43	The method of claim 38, further comprising: placing the set of wafers in an environment of a gas wherein the gas enters each chamber via a pump-out port; and depositing a layer of material on a second side of the first wafer to seal the plurality of pump-out out ports from the second side of the first wafer, wherein each chamber is sealed from an ambient environment.	As noted, instead of evacuating the chambers, the chambers may be filled with a gas and sealed. "Each cavity may have a gas instead of a vacuum." (Column 1 lines 55-56). "The bonded wafer pair 13 and 14 in FIG. 6c may be hermetically sealed with a controlled residual pressure of a specific gas type for optimal thermal, mechanical or other properties rather than simply evacuated for the devices within the chamber." (Column 4 lines 30-34). The method for performing this action is similar to that used to create a vacuum, where the chamber is sealed by depositing a layer of material to seal the plurality of pump-out ports: "Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the

		backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged." (Column 4 lines 9-13).
44	A method for making a wafer-pair with a sealed chamber therebetween, comprising: providing a first wafer and a second wafer; forming one or more pump-out ports through the first wafer;	"Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." (Column 2 line 68 to column 3 line 1). "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m." (Column 3 lines 6-11).
	positioning a first side of the first wafer next to a first side of the second wafer with a sealing ring therebetween,	"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50). "Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60).
	the first wafer, the second wafer and the sealing ring forming a chamber,	"Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si_3N_4 in FIG. 5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO_2 layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37). "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41). "A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50). "Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure." (Column 3 lines 62-63).
	with the pump-out port of the first wafer in fluid	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." Column 2 lines 30-31.

	communication with the chamber; and	And also as shown in Figure 6b.
	plugging the pump out port to seal the chamber.	"Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged." (Column 4 lines 9-13).
	A method according to claim 44 further comprising the step of: making a recess in the first side of the first wafer and/or the first side of the second wafer, wherein the recess is in registration with the chamber.	"Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si_3N_4 in FIG. 5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO_2 layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37). "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41).
46	A method according to claim 44 further comprising the step of: providing one or more devices in or on the first side of the first wafer and/or the first side of the second wafer before the positioning step.	The first metal NiFe (60:40) of a thermocouple is deposited as a 1100 angstrom layer 26 on layer 25 and then first metal layer 26 is patterned with a first mask by ion milling resulting in the layout of FIG. 4d. For the second metal of the thermocouple detectors, a thousand angstrom layer 27 of chromium is deposited on layers 25 and 26. Layer 27 in FIG. 4e is patterned with a second mask by ion milling and wet etching. A layer 28 consisting of 6000 angstroms of Si.sub.3 N.sub.4 is deposited on metal layers 26 and 27, and layer 25, as the top bridge nitride in FIG. 4f. An absorber 29 is deposited on layer 28 of FIG. 4g and patterned with a third mask. Absorber 29 is capped with a layer 30 of Si.sub.3 N.sub.4. Plasma etched vias 31 to metal layer 27 are patterned and cut with the use of a fourth mask, as shown in FIG. 4h. Plasma etched vias 32 in FIG. 4i for the final etch are patterned and cut with the use of a fifth mask. Five hundred angstroms of Cr, 2000 angstroms of Ni and 5000 angstroms of Au are deposited, patterned and lifted off for pad and solder frame metal 33 in FIG. 4j. Passivated leadouts 40 in first metal 26 or second metal 27 pass under the seal ring metal 33 in FIG. 4j. Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG. 4k. There is a KOH etch of the back side of wafer 13 through 90 percent of wafer 13 for port 11 in FIG. 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG.

		4m. (Column 2 line 53 to column 3 line 11).
47	A method according to claim 46 wherein the one or more devices are in registration with the chamber.	"The procedure here has been implemented and resulted in vacuum levels below 10 millitorr of residual pressure as measured by pressure sensors within the cavity." (Column 1 lines 41-44). "Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58). "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20). "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17). "Top cap wafer 14 may have integrated components built in or on the surface in addition to those on the detector wafer 13. Detector wafer 13 having a diaphragm pressure sensor integrated into it, the sealed chamber then forms a vacuum pressure reference. Detector wafer 13 may have infrared bolometer arrays with readout electronics integrated into the wafer. Detector wafer 13 may have moving parts to be sealed in a chamber for other functional purposes." (Column 4 lines 22-30).
48	A method for making a wafer-pair with a sealed chamber therebetween, comprising: providing a first wafer and a second wafer; forming one or more pump-out ports through the first wafer;	"Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." (Column 2 line 68 to column 3 line 1). "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m." (Column 3 lines 6-11).
48b	making a recess in a first side of the first wafer and/or a first side of the second wafer;	"Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si_3N_4 in FIG. 5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO_2 layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37). "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41).
	positioning the first side of the first wafer next to the first side of the second wafer,	"Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60).
	the first wafer and the second wafer forming a	"Cavity 16 is effected by a recess of about 125 microns into wafer 14 having a border 18." (Column 2 lines 21-22).

	chamber that is at least partially defined by the recess,	
	with the pump-out port of the first wafer in fluid communication with the chamber; and	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." Column 2 lines 30-31. Fluid communication of the pump-out port of the first wafer with the chamber is also shown in Figure 6b.
	plugging the pump out port to seal the chamber.	"Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged." (Column 4 lines 9-13).
49	A method for making a wafer-pair with a sealed chamber therebetween, comprising: providing a first wafer having a first side, with one or more bond pads on the first side;	As shown in Figure 4j and also discussed in the specification: "Five hundred angstroms of Cr, 2000 angstroms of Ni and 5000 angstroms of Au are deposited, patterned and lifted off for pad and solder frame metal 33 in FIG. 4j." (Column 3 lines 1-4).
	providing a second wafer; forming one or more bond-pad holes through the second wafer;	"Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si.sub.3 N.sub.4 in FIG. 5b. The wafer 14 is then put in a fixture to allow etching of the outside surface 35 and 36b while protecting the inside 16 and 37b to KOH etch wafer 14 through hole 35 to 90 percent of the way through top cap wafer 14, as shown in FIG. 5c. Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO2 layer 37a in FIG. 5d by buffered oxide etch. Hole 35 is further etched through wafer 14 to layer 37a to complete bond pad hole 35." (Column 3 lines 29-39).
	positioning the first side of the first wafer next to a first side of the second wafer with a sealing ring therebetween;	"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50). "Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60).

	the first wafer, the second wafer and the sealing ring forming a chamber,	"Wafer 14 has a solder adhesion metal and solder ring 15 which matches detector wafer 13, a border 18 forming chamber 16 above detectors 17, and holes 35 through wafer 14 to access the wire bond pads on detector wafer 13." (Column 3 lines 19-23). "A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50). "Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si_3N_4 in FIG. 5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO_2 layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37). "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41). Having shown how the sealing ring may be formed for one embodiment, Figures 6a-6c show that the two wafers may be pressed together and the wafers 13, 14 and sealing ring 18 form a chamber 16.
	the first wafer and second wafer being aligned so that the bond-pad holes are in registration with the one or more bond pads on the first wafer; and	"Wafer 14 has a solder adhesion metal and solder ring 15 which matches detector wafer 13, a border 18 forming chamber 16 above detectors 17, and holes 35 through wafer 14 to access the wire bond pads on detector wafer 13." (Column 3 lines 19-23). Figures 6a-6c show that the bond pad hole 35 is aligned with bond pad 33. Particularly, Figure 6a numbers more portions of the bond pads 33, and the bond pads 33 are clearly in registration with the bond pad hole 35, though the reference numerals on some of the bond pads 33 are not included in each of the Figures.
	the first and second wafers are effectively a bonded together set of wafers.	"Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented. Bonded wafer pair 13 and 14 is put into an E-beam evaporation system for sputter cleaning of the pump-out port 11 surfaces, followed by adhesion layers of 500 angstroms of Ti,

		1000 angstroms of Ni and 500 angstroms of Au. Wafer pair 13 and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum. The wafer pair 13 and 14 is cooled down but the environment about the wafer pair is kept at the desired vacuum. Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged. Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment." (Column 3 line 60 to column 4 line 15).
50	A bonded wafer pair, comprising: a first wafer; a second wafer; the first wafer having one or more pump-out ports through the first wafer;	"Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." (Column 2 line 68 to column 3 line 1). "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m." (Column 3 lines 6-11).
	the first side of the first wafer bonded to a first side of the second wafer via a sealing ring;	"Wafers 13 and 14 are bonded together at solder seal ring 15." (Column 2 lines 15-16). "To begin, the Au solder ring surface 33 of detector wafer 13 is sputter cleaned. The InPb surface of ring 18 of top cap wafer 14 is oxygen plasma cleaned. Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 56-67).
	the first wafer, the second wafer and the sealing ring forming a chamber,	"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50). "Pattern and cut via 35 by plasma etching on outside layers

		36a and 36b and recess 16 on inside layer 37b of Si_3N_4 in FIG. 5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO_2 layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37). "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41). Having shown how the sealing ring may be formed for one embodiment, Figures 6a-6c show that the two wafers may be pressed together and the wafers 13, 14 and sealing ring 18 form a chamber 16.
	with the pump-out port of the first wafer in fluid communication with the chamber; and	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." (Column 2 lines 30-31). Fluid communication of the pump-out port of the first wafer with the chamber is also shown in Figure 6b.
	a plug for plugging the pump out port.	"Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG 6c, to seal vacuum chamber 16 of wafer pair 13 and 14." (Column 4 lines 9-12).
51	A bonded wafer pair according to claim 50 further comprising a recess in the first side of the first wafer and/or the first side of the second wafer, wherein the recess is in registration with the chamber.	"Cavity 16 is effected by a recess of about 125 microns into wafer 14 having a border 18." (Column 2 lines 21-22). "Wafer 14 has a solder adhesion metal and solder ring 15 which matches detector wafer 13, a border 18 forming chamber 16 above detectors 17, and holes 35 through wafer 14 to access the wire bond pads on detector wafer 13." (Column 3 lines 19-23).
52	A bonded wafer pair according to claim 50 further comprising one or more devices in or on the first side of the first wafer and/or the first side of the second wafer.	"The procedure here has been implemented and resulted in vacuum levels below 10 millitorr of residual pressure as measured by pressure sensors within the cavity." (Column 1 lines 41-44). "Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58). "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20). "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17).

		"Top cap wafer 14 may have integrated components built in or on the surface in addition to those on the detector wafer 13. Detector wafer 13 having a diaphragm pressure sensor integrated into it, the sealed chamber then forms a vacuum pressure reference. Detector wafer 13 may have infrared bolometer arrays with readout electronics integrated into the wafer. Detector wafer 13 may have moving parts to be sealed in a chamber for other functional purposes." (Column 4 lines 22-30).
53	A bonded wafer pair according to claim 52 wherein the one or more devices are in registration with the chamber.	"The procedure here has been implemented and resulted in vacuum levels below 10 millitorr of residual pressure as measured by pressure sensors within the cavity." (Column 1 lines 41-44). "Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58). "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20). "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17). "Top cap wafer 14 may have integrated components built in or on the surface in addition to those on the detector wafer 13. Detector wafer 13 having a diaphragm pressure sensor integrated into it, the sealed chamber then forms a vacuum pressure reference. Detector wafer 13 may have infrared bolometer arrays with readout electronics integrated into the wafer. Detector wafer 13 may have moving parts to be sealed in a chamber for other functional purposes." (Column 4 lines 22-30).
54	A bonded wafer pair having a sealed chamber, comprising: a first wafer; a second wafer bonded to the first wafer;	"Wafers 13 and 14 are bonded together at solder seal ring 15." (Column 2 lines 15-16). "To begin, the Au solder ring surface 33 of detector wafer 13 is sputter cleaned. The InPb surface of ring 18 of top cap wafer 14 is oxygen plasma cleaned. Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 56-67).
	one or more pump-out	"Plasma etched vias 32 in FIG 4i for the final etch are

	ports through the first wafer;	patterned and cut with the use of a fifth mask." (Column 2 line 68 to column 3 line 1). "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m." (Column 3 lines 6-11).
	a recess in a first side of the first wafer and/or a first side of the second wafer;	A recess is shown cut into wafer 14 in Figures 5c-5f.
	the first wafer and the second wafer forming a chamber that includes the recess,	"Cavity 16 is effected by a recess of about 125 microns into wafer 14 having a border 18." (Column 2 lines 21-22). "Wafer 14 has a solder adhesion metal and solder ring 15 which matches detector wafer 13, a border 18 forming chamber 16 above detectors 17, and holes 35 through wafer 14 to access the wire bond pads on detector wafer 13." (Column 3 lines 19-23). A chamber including the recess 16 is shown in Figures 6a-c.
	with the pump-out port of the first wafer in fluid communication with the chamber; and	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." (Column 2 lines 30-31). Fluid communication of the pump-out port of the first wafer with the chamber is also shown in Figure 6b.
	one or more plugs for plugging the one or more pump out ports to seal the chamber.	"Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG 6c, to seal vacuum chamber 16 of wafer pair 13 and 14." (Column 4 lines 9-12).
55	A bonded wafer pair, comprising: a first wafer having a first side, with one or more bond pads on the first side;	As shown in Figure 4j and also discussed in the specification: "Five hundred angstroms of Cr, 2000 angstroms of Ni and 5000 angstroms of Au are deposited, patterned and lifted off for pad and solder frame metal 33 in FIG. 4j." (Column 3 lines 1-4).
	a second wafer, with one or more bond-pad holes through the second wafer;	"Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si.sub.3 N.sub.4 in FIG. 5b. The wafer 14 is then put in a fixture to allow etching of the outside surface 35 and 36b while protecting the inside 16 and 37b to KOH etch wafer 14 through hole 35 to 90 percent of the way through top cap wafer 14, as shown in FIG. 5c. Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO2 layer 37a in FIG. 5d by buffered oxide etch. Hole 35 is further etched through wafer 14 to layer

		37a to complete bond pad hole 35." (Column 3 lines 29-39).
	the first side of the first wafer bonded to a first side of the second wafer with a sealing ring therebetween,	"Wafers 13 and 14 are bonded together at solder seal ring 15." (Column 2 lines 15-16). "To begin, the Au solder ring surface 33 of detector wafer 13 is sputter cleaned. The InPb surface of ring 18 of top cap wafer 14 is oxygen plasma cleaned. Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 56-67).
	the first wafer and second wafer being aligned so that the bond-pad holes are in registration with the one or more bond pads on the first wafer; and	Figures 6a-6c show that the bond pad hole 35 is aligned with bond pad 33. Particularly, Figure 6a numbers more portions of the bond pads 33, and the bond pads 33 are clearly in registration with the bond pad hole 35, though the reference numerals on some of the bond pads 33 are not included in each of the Figures.
	the first wafer, the second wafer and the sealing ring forming a chamber.	"Wafer 14 has a solder adhesion metal and solder ring 15 which matches detector wafer 13, a border 18 forming chamber 16 above detectors 17, and holes 35 through wafer 14 to access the wire bond pads on detector wafer 13." (Column 3 lines 19-23). "A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50). "Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si_3N_4 in FIG. 5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO_2 layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37). "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41). Having shown how the sealing ring may be formed for one

		embodiment, Figures 6a-6c show that the two wafers may be pressed together and the wafers 13, 14 and sealing ring 18 form a chamber <u>16</u>.

Respectfully submitted,

R. Andrew Wood et al.

By their attorney,

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Brian N. Tufte, Reg. No. 38,638
CROMPTON, SEAGER & TUFTE, LLC
331 Second Avenue South, Suite 895
Minneapolis, Minnesota 55401-2246
Telephone: (612) 677-9050
Facsimile: (612) 359-9349